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A Hybrid Boost Converter with High Voltage Gain

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Abstract: A hybrid boosting converter (HBC) with collective advantages of regulation capability from its boost structure and gain enhancement from its voltage multiplier structure is proposed in this paper. The new converter incorporates a bipolar voltage multiplier, featuring symmetrical configuration, single inductor and single switch, high gain capability with wide regulation range, low component stress, small output ripple and flexible extension, which make it suitable for front-end PV system and some other renewable energy applications. The operation principal, component stress, and voltage ripple are analyzed in this paper. Performance comparison and evaluation with a number of previous single-switch single-inductor converters are provided. Fuzzy Controlled closed loop of the proposed converter is studied and simulated A 3.5 to 35 V second-order HBC prototypes was built. The experimental results confirm the feasibility of the proposed converter.

Keywords: Hybrid Boost Converter, Bipolar voltage multiplier Continuous conduction mode, Discontinuous conduction Mode.

I. INTRODUCTION

One of the major concerns in the power sector is the day-to-day increasing power demand but the unavailability of enough resources to meet the power demand using the conventional energy sources. Demand has increased for renewable sources of energy to be utilized along with conventional systems to meet the energy demand. Renewable sources like wind energy and solar energy are the prime energy sources which are being utilized in this regard. The continuous use of fossil fuels has caused the fossil fuel deposit to be reduced and has drastically affected the environment depleting the biosphere and cumulatively adding to global warming. Solar energy is abundantly available that has made it possible to harvest it and utilize it properly. Solar energy can be a standalone generating unit or can be a grid connected generating unit depending on the availability of a grid nearby. Thus it can be used to power rural areas where the availability of grids is very low. Another advantage of using solar energy is the portable operation whenever wherever necessary.

In order to tackle the present energy crisis one has to develop an efficient manner in which power has to be extracted from the incoming solar radiation. The power conversion mechanisms have been greatly reduced in size in the past few years. The development in power electronics and material science has helped engineers to come up very small but powerful systems towith stand the high power demand. But the disadvantage of these systems is the increased power density. Trend has set in for the use of multi-input converter units that can effectively handle the voltage fluctuations. But due to high production cost and the low efficiency of these systems they can hardly compete in the competitive markets as a prime power generation source. The constant increase in the development of the solar cells manufacturing technology would definitely make the use of these technologies possible on a wider basis than what the scenario is presently.

In recent years, the rapid development of renewable energy system calls for new generation of high gain dc/dc converters with high efficiency and low cost. The front end of "Plug and Play" PV system usually demands step-up converter which is capable of boosting the voltage from 35 to 380Vwith regulation capability due to the low terminal voltage and the requirement of MPPT tracking function for single PV panel. Considering a wind farm with internal medium-voltage dc (MVDC)-grid system, a MVDC converter able to boost the voltage from 1–6 to 15–60 kV is required to link the output of generator-facing rectifier to the MVDC line. Some other energy storage systems such as fuel cell powered system also require high-gain dc/dc converter due to their low voltage level at storage side. In order to achieve high voltage conversion ratio with high efficiency, many high gain enhancement techniques were investigated in the previous publications. Among them, switched capacitor structure, tapped/coupled inductor-based technique, transformer-based technique, voltage multiplier structure or combinations of them attracted significant attentions. Each technology has its unique advantages and limitations. The switched capacitor dc–dc converter can achieve high efficiency but has pulsating current and poor regulation capability. Introduction of resonant switched-capacitor converter can

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alleviate the pulsating current but does not solve the regulation issue. The tapped-inductor and transformer facilitates gain boosting function but requires snubber circuit to handle leakage problem. The combination of above technologies usually yields promising circuit features but with excessive number of components. In this paper, gain enhancement technology based on modification of traditional boost converter while maintaining single inductor and single switch is investigated, targeting at simplifying the circuit design, reducing the cost, satisfying the demands of normal high gain applications, and facilitating mass production.

II. CONVENTIONAL CONVERTERS

The idea of gain enhancement from a boost converter started from quadratic boost. It achieved higher voltage gain with a single switch, yet introduced high component voltage stress. Nevertheless, this converter motivated high gain converter development follow on.

Many gain extension methods of boost converter by adding only diodes and capacitors were investigated in the past. The method of combining boost converter with traditional Dickson multiplier and Cockcroft–Walton multiplier to generate new topologies were proposed in, such as topologies in Fig. 2.1 and 2.2

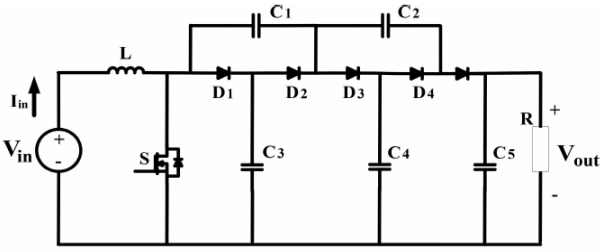

Fig 2.1.Boost + Dickson multiplier

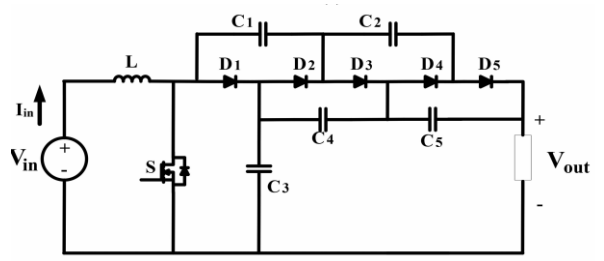

Fig 2.2Boost + Cockcroft–Walton multiplier

Air core inductor or stray inductor was used within voltage multiplier unit to reduce current pulsation in. An elementary circuit employing the super lift technique was proposed in and extended to higher gain applications such as Fig. 2.3. Its counterpart of negative output topology and double outputs topology were proposed and discussed. The concept of multilevel boost converters was investigated and the topology of Fig. 2.4 was given as central source connection converter. Besides, two switched capacitor cells were proposed and numerous topologies were derived by applying them to the basic PWM dc–dc converters. Typical topologies are shown as Fig. 2.5 and 2.6.

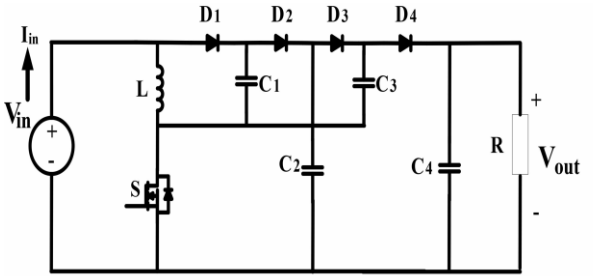

Fig 2.3superlift with elementary circuit

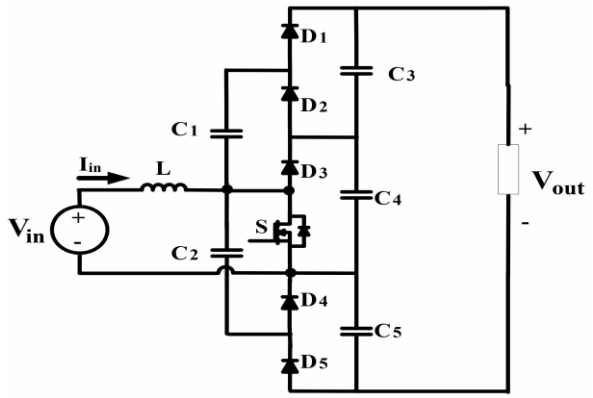

Fig 2.4 central source multilevel boost converter

Inspired by the above topologies, a new hybrid boosting converter (HBC) with single switch and single inductor is proposed by employing bipolar voltage multiplier (BVM) in this paper. Compared with other listed topologies in Figure, the proposed converter decreases the voltage rating of output filter capacitor and exhibits the nature interleaving operation characteristics. Compared with the converter in Fig. 2.4, the proposed converter has smaller output ripple and higher components utilization rate with respect to conversion ratio. Some interleaving technologies for ripple reduction and power expansion were reported in the literature, but these methods are normally based on circuit branch expansion which requires more components. The proposed topology has achieved smaller ripple with single switch and single inductor while maintaining high voltage gain.

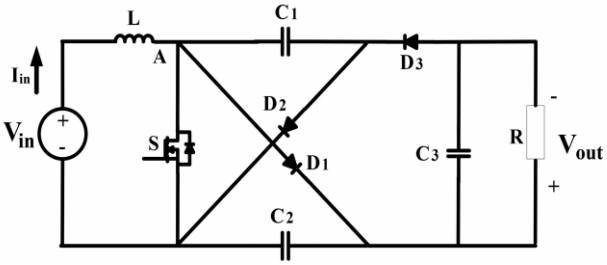

Fig 2.5 central source multilevel boost converter

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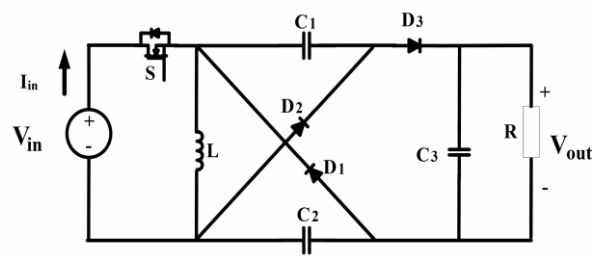

Fig 2.6 Cuk derived

Recently, many more structures achieving higher gain were also reported, but they adopted at least two inductors or switches, or some are based on tapped inductor/transformer, which may complicate the circuit design and increase cost.

This paper is organized as follows: chapter 4 gives the general topology of basic HBC and discusses the operation principal. The steady-state analysis is given in Section 5. Circuit performance analysis such as components stress, voltage ripple and circuit comparison are presented in Section 6. Simulation and experimental results are given in Section 7 and the conclusion is drawn in Section 8.

III.PROPOSED CONVERTER

The proposed HBC is shown in Fig. 2. There are two versions of HBC, odd-order HBC and even-order HBC as shown in Fig. 2(a) and (b). The even-order topology integrates the input source as part of the output voltage, leading to a higher components utilization rate with respect to the same voltage gain. However, they share similar other characteristics and circuit analysis method. Therefore, only even-order topology is investigated in this paper.

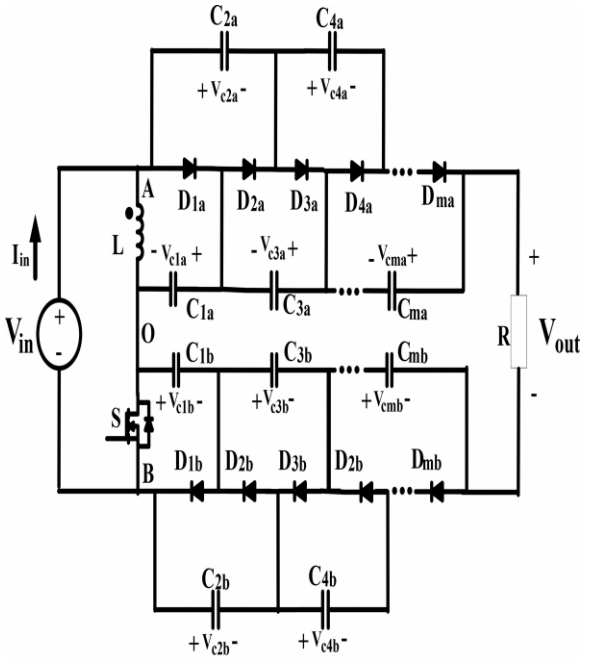

Fig3.1 Even Order HBC

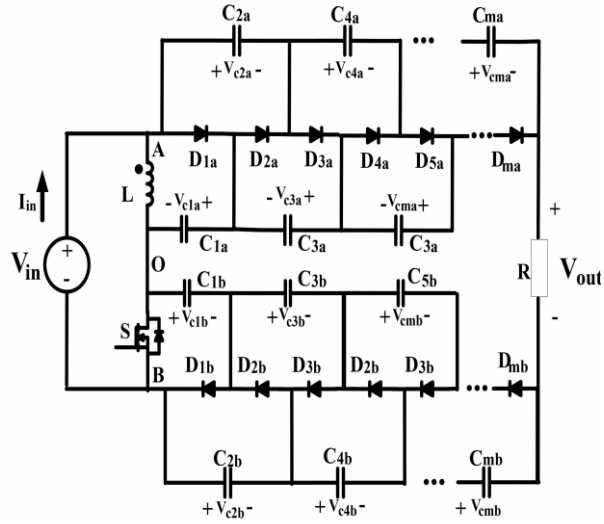

Fig3.2 Odd order HBC

3.1 Inductive Switching Core

In a HBC topology, the inductor, switch and input source serve as an "inductive switching core," shown as Fig.3.3. It can generate two "complimentary" PWM voltage waveforms at port AO and port OB. Although the two voltage waveforms have their individual high voltage level and low voltage level, the gap between two levels is identical, which is an important characteristic of inductive switching core for interleaving operation

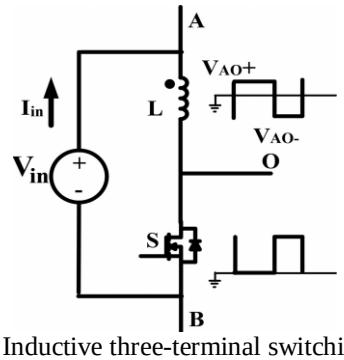

Fig.3.3 Inductive three-terminal switching core

3.2 BVM

A BVM is composed of a positive multiplier branch and a negative multiplier branch, shown in Fig.3.4 and 3.5. Positive multiplier is the same as traditional voltage multiplier while the negative multiplier has the input at the cathode terminal of cascaded diodes, which can generate negative voltage at anode terminal, shown in Fig. 3.5. By defining the high voltage level at input AO as V_{OA+}, the low voltage level as V_{OA-}, and the duty cycle of high voltage level as D, the operational states of the even-order positive multiplier is derived as Fig. 5 and illustrated as following:

a).State 1 [0, DTs]:

When the voltage at port AO is at high level, diodes*Dia* ($i = 2k - 1, 2k - 3 \ldots 3, 1$) will be conducted consecutively.

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Each diode becomes reversely biased before the next diode fully conducts. There are K sub states resulted as shown in Fig. 5(a).Capacitor *Cia* (i = 2, 4 . . . 2k) are discharged during this time interval. Assuming the flying capacitors get fully charged at steady state and diodes voltage drop are neglected, the following relationship can be derived:

$$V_{c1a} = V_{AO+} \quad (1)$$
$$V_{cia} = V_{c(i+1)a} (i = 2, 4, 6, ..., 2k - 2) \quad . (2)$$

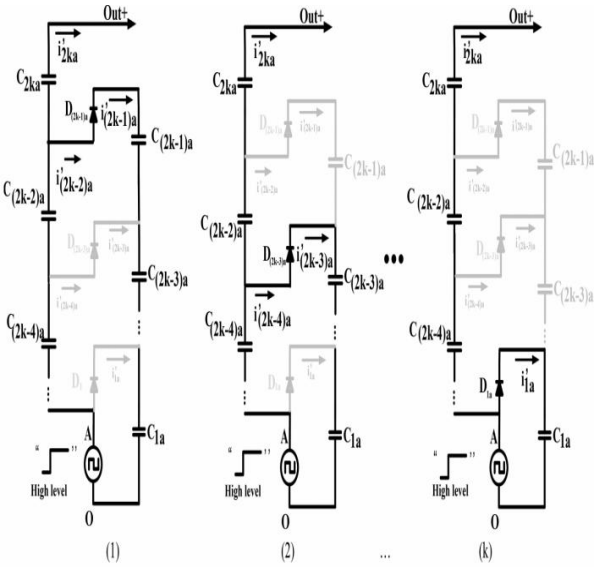

Fig 3.4 Operation modes of even-order BVM positive branch. (a) State 1[0, DTs]

b).State 2[dTs, Ts]:

When the voltage at port AO steps to low level, diode *D*2*k a* is conducted first, shown as Fig. 5(b)-(1). Then the diodes *Dia* (i = 2, 4, . . . 2k − 2) will be turned on one after another from high number to low. Each diodewill be turned on when the previous one becomes blocked. Only diode D_{2ka} is conducted for the whole time interval of [0, dTs], since capacitor $C_{(2k-1)a}$ has to partially provide the load current during the whole time interval. Even though not all the diodes are conducted and blocked at the same time, the flying capacitors still have the following relationship by the endof this time interval:

$$V_{c2a} = V_{c1a} - V_{AO} \quad (3)$$
$$V_{cia} = V_{c(i+1)a} (i = 3, 5, 7, . . . , 2k - 1). \quad (4)$$

According to charge balance principal, the total amount of electrical charge flowing into capacitors *Cia* (i = 2, 4, . . . 2k) should equal to that coming out from them in a switching period at steady state, therefore

$$\sum_{i=1}^{k} \int_{0}^{DT_S} i'_{2ia} dt = \sum_{i=1}^{k} \int_{DT_S}^{T_S} i_{2ia} dt. \quad (5)$$

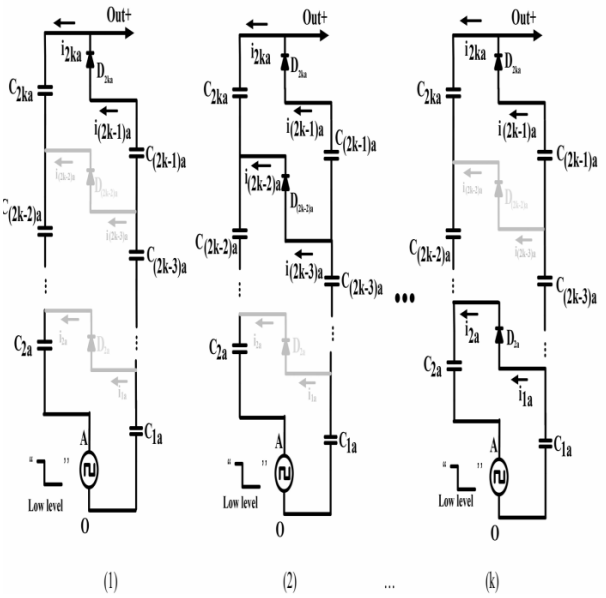

Fig3.5 Operation modes of even-order BVM positive branch. (b) State 2[DTs, Ts].

Thus, the capacitor group C_{ia} (i = 2, 4 . . . 2k) can be replaced by an equivalent capacitor $C_{2a(eq)}$.The diode group D_{ia} (i = 2, 4 . . . 2k) which provides the charging path for *C*2*a*(*eq*) is equivalent to a single diode $C_{2a(eq)}$. Similarly, the capacitor group C*ia* (i = 1, 3, . . . 2k − 1) can be replaced by an equivalent capacitor $C_{1a(eq)}$ and diode group *Dia* (i = 1, 3, . . . 2k − 1) by $D_{1a(eq)}$. The final equivalent even-order positive multiplier branch is given as Fig. 6(a). A similar analysis yields the equivalent negative multiplier branch asshown in Fig. 6(b). According to (1)–(4), the voltage of equivalent capacitors $C_{1a(eq)}$,$C_{2a(eq)}$ can be expressed as following:

$$V_{c2a(eq)} = k(V_{AO+} - V_{AO-}) \quad (6)$$
$$V_{c1a(eq)} = (k - 1)(V_{AO+} - V_{AO-}) + V_{AO+}. \quad (7)$$

For the negative branch shown in Fig. 6(b), the following results can be obtained based on similar analysis:
where *V*OB+ is the high voltage level of input port OB and *V*OB− is the low voltage level.

$$Vc2b(eq) = k(V_{OB+} - V_{OB-}) \quad (8)$$
$$V_{c1b(eq)} = (k - 1)(V_{OB+} - V_{OB-}) + V_{OB+} \quad (9)$$

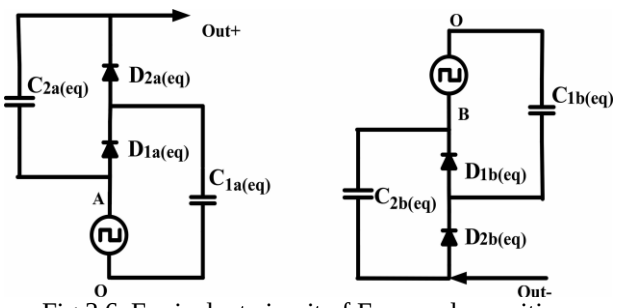

Fig 3.6. Equivalent circuit of Even-order positive multiplier and Even-order negative multiplier

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IV. DESIGN EQUATIONS

Equivalent Capacitance Derivation: Assuming capacitors C_{ia} (i = 1, 2, 3, . . . 2k) have the same capacitance C, in order to derive the equivalent capacitance of $C_{2a(eq)}$ and $C_{1a(eq)}$ in expression of C, a voltage ripple-based calculation method is proposed in this section. Assuming the peak to peak voltage ripple of the flying capacitors can be expressed as ΔV_{cia} (i = 1, 2, 3 . . . 2k), the ripple of equivalent capacitor $C_{2a(eq)}$ isΔV , the following relationship can be approximated:

$$\Delta V = \Delta V_{c2a} + \Delta V_{c4a} + \ldots . \Delta V_{c2ka} \qquad (10)$$

In Fig. 5, assuming the average current of i'_{ia} (i = 1, 2, 3 . . . 2k) during [0, dTs] is (i = 1, 2, 3 . . . 2k) $\overline{i'_{2ia\,(\text{on})}}$ and the average current of i_{ia} (i = 1, 2, 3 . . . 2k) during [dTs, Ts] is $i'_{ia(off)}$ (i = 1, 2, 3 . . . 2k), according to charge balance of capacitors C_{ia} (i = 2, 4 . . . 2k), it can be derived that

$$\overline{i'_{ia\,(on)}} DTS = \overline{i_{ia(\text{off})}} D'TS \ (i = 2, 4, \ldots 2k). \qquad (11)$$

At the same time, state 1 gives

$$\overline{i'_{ia\,(on)}} = \overline{i'_{(i+1)a(\text{on})}} \ (i = 2, 4, \ldots 2k - 2) \qquad (12)$$

State 2 gives

$$\overline{i_{ia(\text{off})}} = \overline{i_{(i+1)a(\text{off})}} (i = 1, 3, \ldots 2k - 3). \qquad (13)$$

Based on the (11)–(13), the following relationship can be obtained:

$$\overline{i_{2a(\text{off})}} = \overline{i_{4a(\text{off})}} = \ldots \overline{i_{(2k-4)a(\text{off})}} = \overline{i_{(2k-2)a(\text{off})}} = \overline{i_{(2k-1)a(\text{off})}} . \qquad (14)$$

Based on charge balance of capacitor C_{2ka} , it can be derived that

$$\overline{i_{2(k-1)a(\text{off})}} D'TS = I_{oTS} \qquad (15)$$

$$\overline{i_{2ka(\text{off})}} DTS = \overline{i_{2ka(\text{on})}} DTS = I_o DT_S \qquad (16)$$

where $I = \frac{Vout}{R}$

According to KCL in Fig. 5(b), voltage ripple of capacitors Cia (i = 2, 4 . . . 2k) can be obtained

$$C\Delta V_{c2a} = (\overline{i_{2ka(\text{off})}} + \overline{i_{2k-2a(\text{off})}} + \ldots \overline{i_{4a(\text{off})}} + \overline{i_{2a(\text{off})}}) D'T_S$$
$$C\Delta V_{c4a} = (i_{2ka(\text{off})} + i_{2k-2a(\text{off})} + \ldots . i_{4a(\text{off})})$$
$$D'T_S \, C\Delta V_{c2ka} = \overline{i_{2ka(\text{off})}} \, D'TS \qquad (17)$$

where $D' = 1 - D$.
Based on the equations from (14) to (16), the equation group (17) can be reduced to the following expression:

$$C\Delta V_{c2a} = (k - 1 + D) I_O T_S$$
$$C\Delta V_{c4a} = (k - 2 + D) I_O T_S$$
.
.
.
.
$$C\Delta V_{c2ka} = (0+D) I_O T_S. \qquad (18)$$

Substituting (10) to (18), the following equation is derived:

$$C\Delta V = \left(\frac{k(k-1)}{2} + kD\right) \quad I_O T_S . \qquad (19)$$

Meanwhile, the following equation can be derived based on discharging stage of equivalent capacitor $C_{2a(eq)}$:

$$C_{2a(eq)} \Delta V = I_O D T_S \qquad (20)$$

Based on (19) and (20), the equivalent capacitor $C_{2a(eq)}$ can be expressed

$$C_{2a(eq)} = \frac{2D}{k(k-1+2D)} C. \qquad (21)$$

Similarly, in order to derive the equivalent capacitance of $C1a(eq)$, the following equation can be derived:

$$C\Delta V_{c1a} = kI_O T_S$$
$$C\Delta V_{c3a} = (k - 1) I_O \, T_S$$
$$C\Delta V_{c2(k-1)a} = I_O T_S \qquad (22)$$

At the same time, the following equation exists:

$$C_{1a(eq)} \Delta V = I_O T_S \qquad (23)$$

Where $\Delta V\_ = \Delta V_{c1a} + \Delta V_{c3a} + \ldots \Delta V_{c(2k-1)a}$.
Therefore, the expression of $C_{1a(eq)}$ is obtained

$$C_{1a(eq)} = \frac{2}{(k+1)k} C. \qquad (24)$$

Because of the symmetry, the equivalent capacitance $C_{1b(eq)}$ and $C_{2b(eq)}$ is given as following:

$$C_{1b(eq)} = \frac{2}{(k+1)k} C \qquad (25)$$

$$C_{2b(eq)} = \frac{2D'}{k(k-1+2D')} C. \qquad (26)$$

V. MODES OF OPERATION

Based on the simplification method discussed in previous section, the general even-order HBC in Fig. 2(b) can be simplified to an equivalent HBC circuit, shown as Fig. 8. Careful examination of the topology indicates that the two "boost" like sub circuits are intertwined through the operation of the active switch S. The total output voltage of HBC is the sum of the output voltage of two boost subcircuits plus the input voltage. Three operation states are described as Fig. 7.

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Mode: 1[0, DTs]

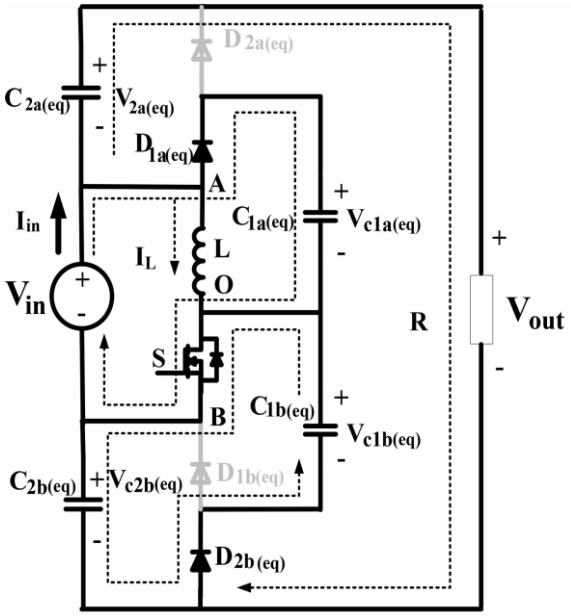

Fig5.1 HBC mode 1

In Fig. 7(a), switch S is turned on and diodes $D_{1a(eq)}$, $D_{2b(eq)}$ conduct while diodes $D_{2a(eq)}$ and $D_{1b(eq)}$ are reversely biased. The inductor L is charged by the input source. Meanwhile, capacitor $C_{1a(eq)}$ is charged by input source and capacitor $C_{2b(eq)}$ is charged by capacitor $C_{2b(eq)}$. At this interval, the following equations can be derived based on the inductive switching core analysis:

$$4\,V_{AO+} = Vin \qquad (27)$$

$$V_{OB-} = 0. \qquad (28)$$

Mode 2:[DTs,(D + D1)Ts]

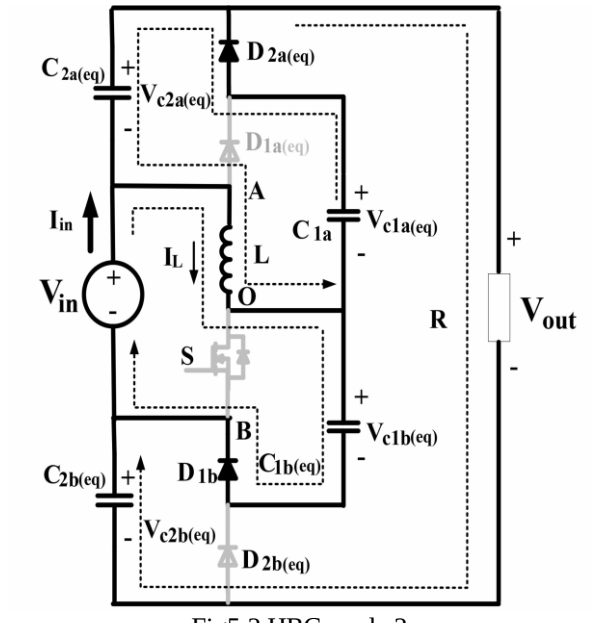

Fig5.2 HBC mode 2

As illustrated in Fig.5.2, when *S* is turned off, the inductor current will free wheel through diodes $D_{2a(eq)}$ and$D_{1b(eq)}$.The inductor is shared by two charging boost loops. In the top loop, capacitor $C_{1a(eq)}$ is releasing energy to capacitor $C_{2a(eq)}$ and load at the same time. In the bottom loop, input source charges capacitor $C_{1b(eq)}$ through the inductor L. During this time interval, voltage generated at AO and OB is expressed as following based on inductor balance principal:

$$V_{AO+} = -Vin\,\frac{D}{D'} \qquad (29)$$

$$V_{OB+} = \frac{Vin\ (D + D1)}{D1} \qquad (30)$$

Mode 3: [(D + D1)Ts, Ts]

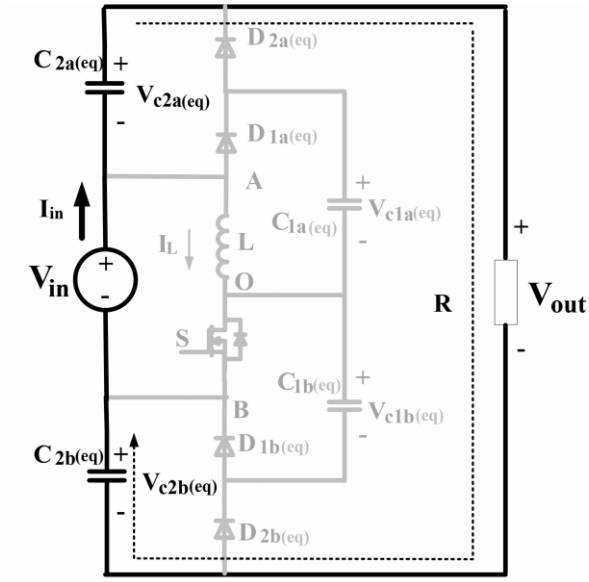

Fig 5.3 HBC mode 3

Under certain conditions, the circuit will work under DCM operation mode, thus the third state in Fig. 5.3 appeals. At this state, the switch S is kept off. The inductor current has dropped to zero and all the diodes are blocked. The capacitor $C_{2a(eq)}$ and $C_{2a(eq)}$are in series with input source to power the load. During this time interval, voltage generated at port AO is zero while at OB is *V*in.

VI. STEADY-STATE ANALYSIS

6.1 Voltage Gain Derivation In Ccm Mode

In steady state, the CCM mode operation waveforms are given as Fig. 9(a). The waveforms of V_{AO} and V_{OB} are presented based on operation principal analysis previously. Under CCM condition, $D_1 = 1- D = D'$. Based on (6) and (8), the equivalent voltage of $C_{2a(eq)}$ and $C_{2b(eq)}$ is obtained as

$$V_{c2b(eq)} = k\frac{Vin}{D'} \qquad (31)$$

$$V_{c2a(eq)} = k\,\frac{Vin}{D'}. \qquad (32)$$

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Therefore, the voltage ratio of a general 2kth-order HB shown in Fig. 2(b) is derived as following:

$$\frac{Vout}{Vin}=1+2k\frac{1}{D'} \quad (33)$$

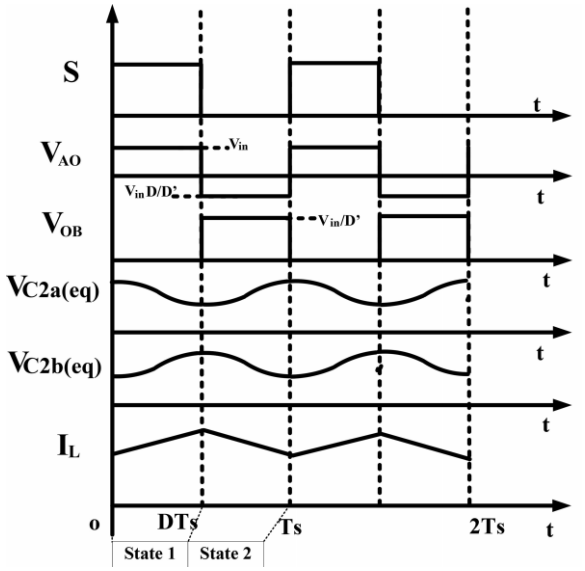

Fig 6.1CCM mode wave form

6.2 Voltage Gain Derivation In DCM Mode

Under DCM operation mode, the waveforms of voltage at input port AO, OB are shown in Fig. 6.2. Based on (6) and (8), the voltage gain can be expressed as

$$Vout = Vin + 2kVin\frac{D+D'}{D}. \quad (34)$$

In Fig. 6.1, the inductor current can be expressed as following during state 2:

$$I_L = I_{D2a(eq)} + I_{D1b(eq)}. \quad (35)$$

According to charge balance principal of the circuit

$$I_{D2a(eq)} = I_{D1b(eq)} = I_O \quad (36)$$

where $I_{D2a(eq)}$ and $I_{D1b(eq)}$ are the average current in the whole switching period.
As current waveforms of $I_{D2a(eq)}$ and $I_{D1b(eq)}$ should both have triangle shape, they will share same peak current value, which is half of the inductor peak current. Therefore

$$I_{D2a(eq)p-p} = I_{D1b(eq)p-p} = \frac{1}{2}\frac{Vin}{L}DT_S \quad (37)$$

The average current of $I_{D2a(eq)}$ in a switching period is I_O , thus

$$\frac{1}{2}\ D1Ts\ \frac{1}{2}\frac{Vin}{L}DTs\frac{1}{Ts}=Io \quad (38)$$

This can be simplified to

$$D1 = \frac{4IOL}{Vin\ Ts\ D} \quad (39)$$

Substituting (37) to (32), the following equation can be derived:

$$Vout = Vin + 2k\ (Vin + \frac{Vin^2 D^2 Ts}{4\ IoL}) \quad (40)$$

Solving the (38) gives the voltage gain in DCM mode

$$\frac{Vout}{Vin}=\frac{2K+1+\sqrt{(2K+1)^2+K^2\frac{2D^2Ts}{L}}}{2}. \quad (41)$$

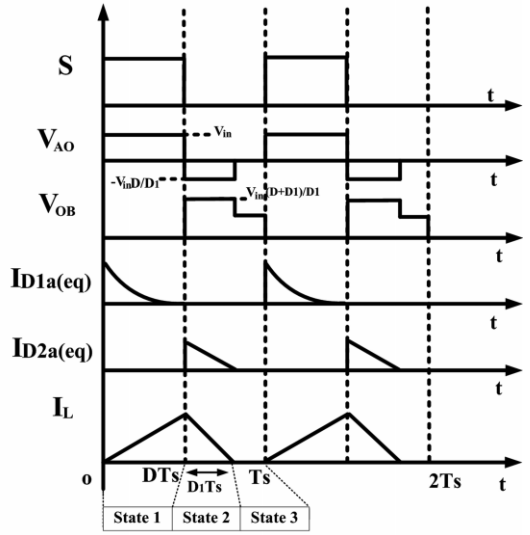

Fig 6.2 DCM mode

6.3 BRM Mode Analysis

In order to derive boundary condition for CCM and DCM mode, the average power balance is used

$$Vin\ (I_L + I_{D1a(eq)}) = Vout\ I_O \quad (42)$$

where $I_{D1a(eq)}=I_O = \frac{Vout}{R}$
Thus, the average current of I_L under CCM condition is

$$I_L = \frac{2K}{D'}\frac{Vout}{R} \quad . (43)$$

The current ripple of inductor is

$$\Delta i_L = \frac{Vin}{2L}DT_S. \quad (44)$$

Therefore, the CCM condition is

$$\frac{2K}{D'}\frac{Vout}{R} > \frac{Vin}{2L}DT_S \quad . (45)$$

The criteria can be rearranged as

$$\frac{2L}{RTs} > \frac{DD'}{2K(D'+2K)}^2 = K_{crit}\ (D) \quad (46)$$

The curves of Kcrit(D) with k = 1, 2, 3 are shown in Fig. 10. It can be seen that when the voltage multiplier stage increases, it is easier to achieve CCM when other parameters are fixed.

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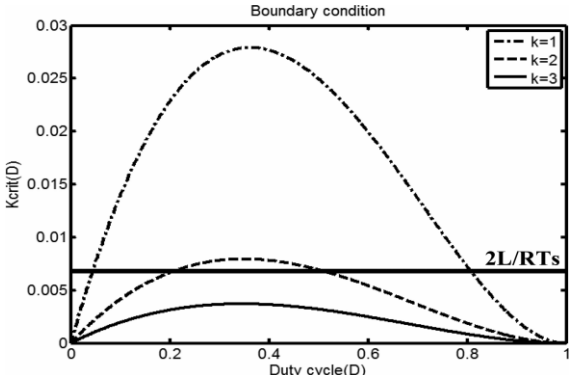

Fig 6.3 *K*crit(*D*) with variation of K

VII. CLOSED LOOP HYBRID BOOST CONVERTER

7.1 Introduction

The performance of Hybrid Boost converter can be improved further by a closed loop control. Even though the open loop Hybrid Boost Converter is simple, it is not capable of giving an accurate output. Therefore closed loop Hybrid boost converter using PI and Fuzzy is studied and simulated and the performance are analyzed.

7.2 Open Loop and Closed Loop System

There are basically two different types of control systems, open loop system and closed loop system.

Fig 7.1 Open Loop control system

Fig 7.1 shows a simple open loop control system. In open loop control system, when an input signal direct the control element to respond, an output will be produced. The open loop system achieves an out state at some equilibrium (steady state) point. It is also called as a non feedback controller, and is a type of controller that computes its input into a system using only the current state and its model of system. A characteristic of the open loop controller is that it does not use feedback to determine if its output has achieved the desired goal of the input. This means that the system does not observe the output of the processes that is controlling .Consequently a true open loop system cannot engage in machine learning and also cannot correct any errors that it could make. It also may not compensate for disturbance in the system.

Sometimes, we may use the output of the control system to adjust the input signal. This is called feedback. Feedback is a special feature of a closed loop system. A closed loop systems compares the output with the expected result or command status, and it takes appropriate control action to adjust the input signal. A well designed feedback system can often increase the accuracy of the output fig 7.2 shows a closed loop system. The output is feed backed to the input. The desired output is given as preset value. The difference between preset signal and output is calculated. It is called error; this error signal is used to control the process.

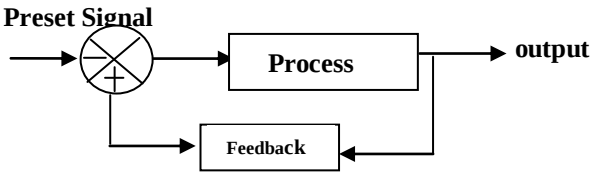

Fig 7.2 Closed loop system

7.3 Closed loop HBC

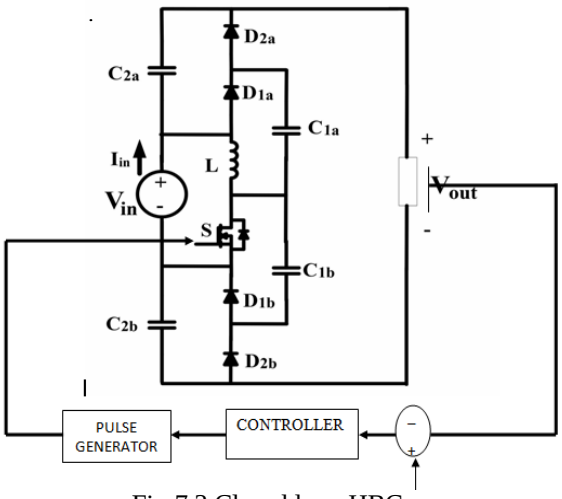

Fig 7.3 Closed loop HBC

The closed loop HBC consists of a feedback system comprising of a controller and a pulse generation unit. Different type of controllers is used such as Propotional Controller, Integral Controller, Fuzzy controller and combinations of these. The MATLAB simulation of open loop HBC and closed loop HBC using PI and Fuzzy Controller are simulated and results are obtained.

7.3.1 PI Controller

Combination of Propotional controller and integral controller constitutes PI controller. At present PI controller is widely adopted in industrial application due to its simple structure, easy design and low cost. The use of propotional integral controller improves transient response. The PI controller will also eliminate forced oscillation and steady state error resulting in operation of P controller alone respectively. Despite these advantages, the PI controller fails when the controlled object is highly non linear and uncertain

The closed loop HBC controlled using PI controller has simulated using MATLAB Simulink software. The Control logic of PI controller is shown in figure 7.4. The error between output voltage of converter (Vout) and desired output voltage (Vref) is calculated and given as input to PI controller.

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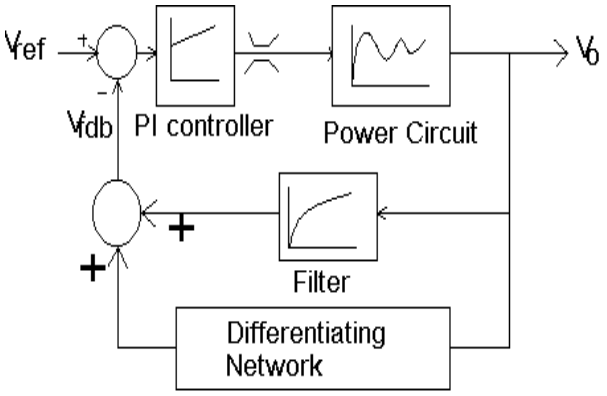

Fig 7.4 Control logic of PI controller

The controller computes a signal equal to the propotional gain (Kp) times the magnitude of the error plus the integral gain (Ki) times the integral of the error. It is then compared with repeating sequence to generate gate logic of converter. It has found that more precise output , reduced overshoot and reduced steady state error in output. But there was no rapid error correction and ripple content not reduced much. Therefore the PI controller is replaced by a Fuzzy Logic controller.

7.3.2 Fuzzy Controller

The Fuzzy Controller is a controller which work based on a Fuzzy logic. Fuzzy logic is an approach to computing based on "degree of truth" rather than the usual "true or false" (0 or 1) Boolean logic. It allows decision making with estimated values under incomplete or uncertain information. The input variables in a fuzzy control system are in general mapped by sets of membership functions similar to this, known as "fuzzy sets". The process of converting a crisp input value to a fuzzy value is called "fuzzification".

A control system may also have various types of switch, or "ON-OFF", inputs along with its analog inputs, and such switch inputs of course will always have a truth value equal to either 1 or 0, but the scheme can deal with them as simplified fuzzy functions that happen to be either one value or another.

Given "mappings" of input variables into membership functions and truth values, the microcontroller then makes decisions for what action to take, based on a set of "rules", each of the form

Consider an example showing the speed variation in classical set and fuzzy sets. In the classical set , any speed can only be categorized into one subset, LOW ,MEDIUM, or HIGH,and the boundary is crystal clear. But in Fuzzy set such as shown in the figure below, this boundary becomes smooth and vague. One speed can be categorized into two or may be even three subsets simultaneously. A fuzzy set allows a member to have a partial degree of membership between 0and 1 including that.

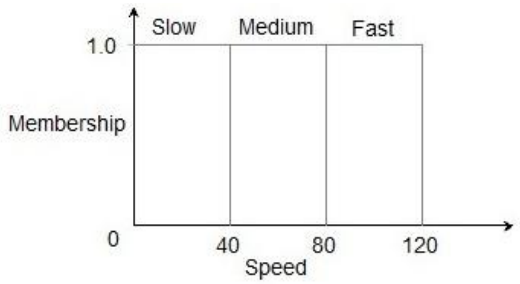

Fig7.5 classical set

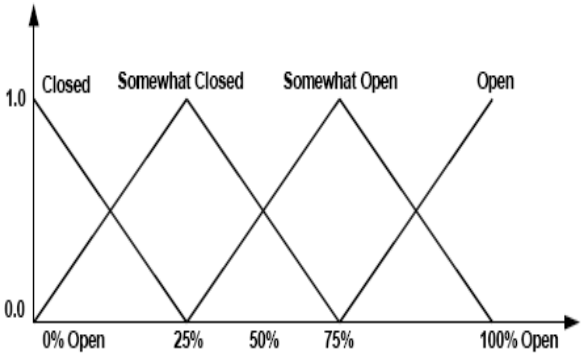

Fig 7.6 Fuzzy Set

A fuzzy inference system (FIS) is a system that uses fuzzy set theory to map inputs (*features* in the case of fuzzy classification) to outputs (*classes* in the case of fuzzy classification).The basic block diagram of Fuzzy Inference System is shown in the block diagram below. It consist of a fuzzification unit, rule base, data base, a decision making unit and a defuzzification unit.

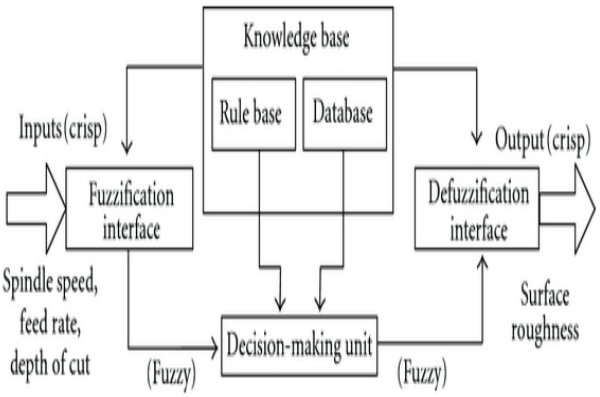

Fig 7.7 Fuzzy Inference System

The function of each block is as follows:

- Knowledge Base: It contains the rule and datas that guide the system behavior
- Rulr base: It contains a number of fuzzy IF-THEN rules. FIS uses "IF..THEN…" statements and connectors "AND" or "OR" to make necessary decision rules. Fuzzy uses user-supplied human languages rule.

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- Data Base: It defines the membership function of fuzzy set used in fuzzy rules
- Fuzzification unit.; It transforms crisp input data into fuzzy so that it may handled in fuzzy reasoning process i.e.;fuzzy set of any kind
- Decision making unit: It perform the inference operation on rules.
- Defuzzification unit: It transforms fuzzy value to crisp value that constitutes the output of FIS

7.3.3 Input and output Membership functions

In order to control two outputs of the closed loop HBC, fuzzy logic controller are used. It has two input membership functions and single output membership functions. The input and input 1 are the error and change in error to the fuzzy.

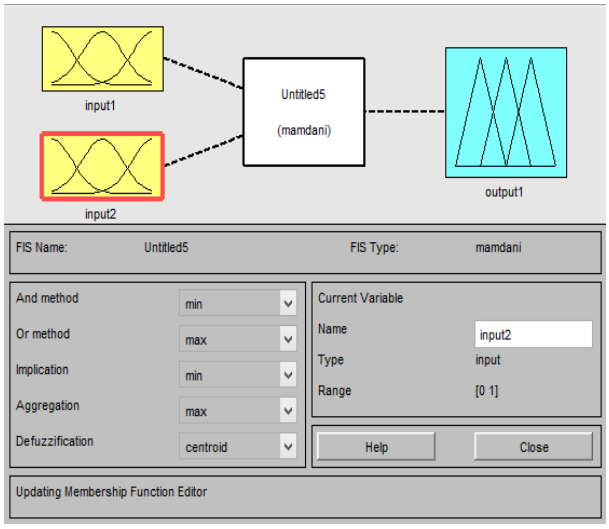

Fig 7.7 Membership functions

7.3.4 Fuzzification and Defuzzification

For each input and output variable selected, we define two or more membership functions (MF), normally three but can be more. We have to define a qualitative category for each one of them, for example: low, normal or high. The shape of these functions can be diverse but we will usually work with triangles and trapezoids (actually usually pseudo-trapezoids). For this reason we need at least three (for triangles) or four (for trapezoids) points to define one MF of one variable

Next question to be solved is how to fuzzificate all the real values of the variable x. First, for a given value of x, for example x_n which can belong to one or more MF we calculate the y value for each of the MF/s which x_n belong. This y value has to be between 0 and 1.

For example: Consider three MF: low, normal and high and a given value of x_n, then the degrees of membership to each MF (y values) for x_n can be, for example: 0.6 for the MF low and 0.4 for the MF normal (see Figure 6). Likewise, we can fuzzificate all the values of any variable. Any of the values will belong to at least one MF with a certain degree of membership.

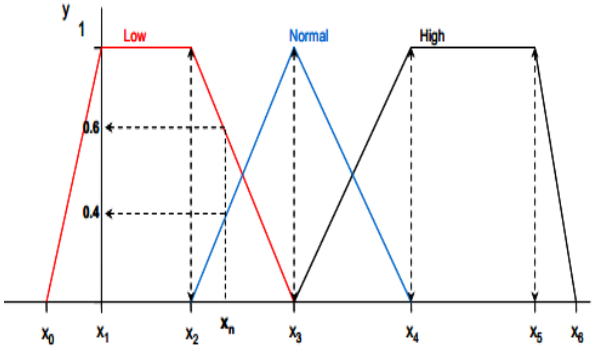

Fig 7.8. Example of the three MF for a given input

Defuzzificztion: The MFs of the output have always the same shape and configuration in our risk model: the risk vof any problem has the same ranks for the MFs of the output: low, normal and high, and always without overlapping.

Figure 7.9 shows the shape of each MF of the output variable (risk on any problem considered in the risk model).

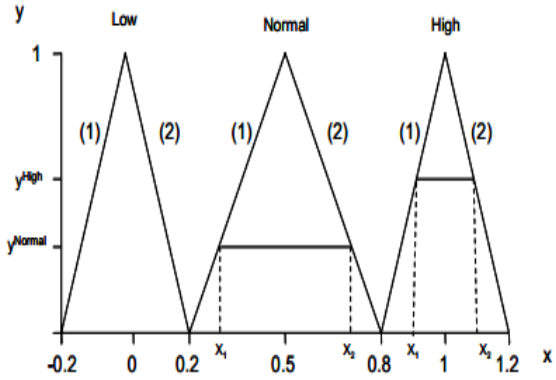

Fig7.9 MFs of the risk of any problem within the risk model

VIII. MATLAB SIMULATION AND RESULTS

8.1 Introduction

The MATLAB Simulink is a software package for modeling, simulating and analyzing dynamical system. It supports linear and non-linear systems, modeled in continuous time, sampled time or a hybrid of the two. The simulation result can be put iin MATLAB workspace for processing and visualization. The MATLAB simulation of conventional Voltage multiplier, Open loop HBC, Closed Loop HBC using PI and Fuzzy Controller is carried out. The result of simulation is included in this chapter.

8.2 MATLAB/Simulink Model of Voltage Multiplier

Conventional voltage multiplier simulation is shown in figure 8.1 with input voltage 350v

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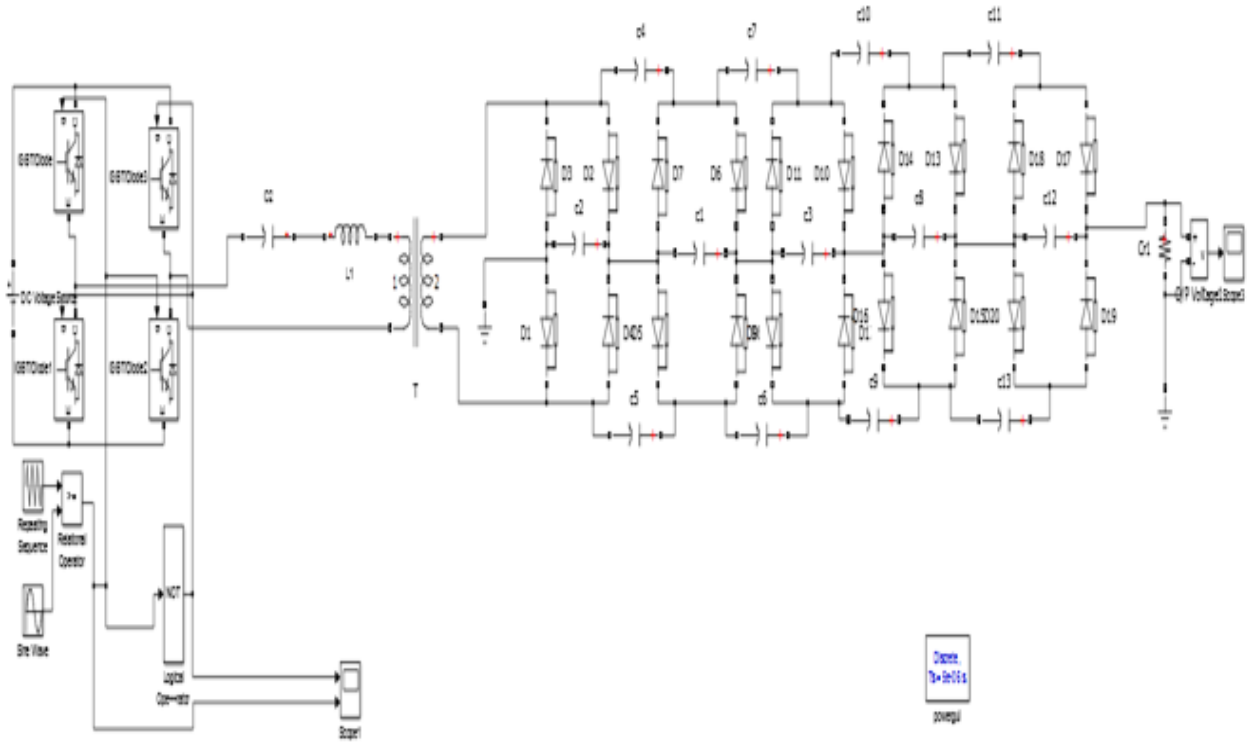

Fig8.1 Simulink Model of Conventional Voltage Multiplier

8.3 Simulink Model of Open Loop HBC

The simulink model of open loop HBC is shown in figure 8.2. The input is 35 V

8.4 Simulink Model of Closed Loop HBC using PI controller

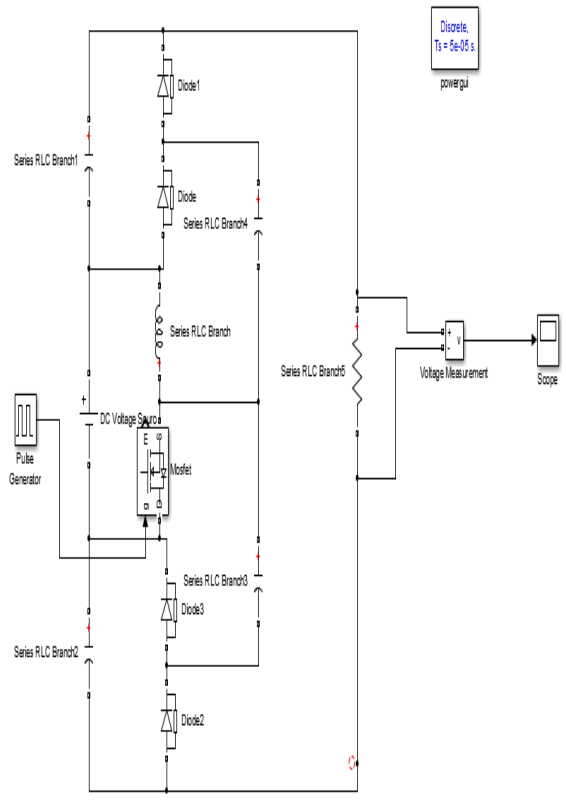

Fig 8.2 open loop HBC

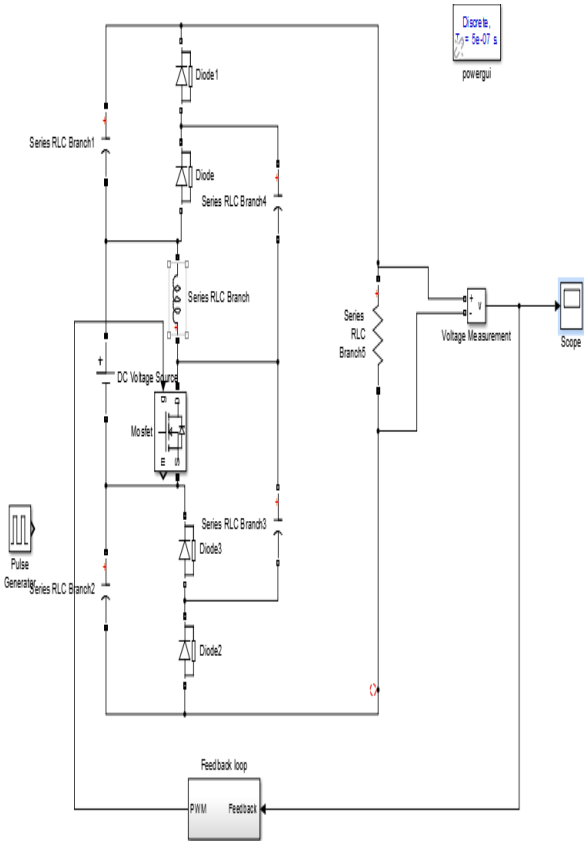

Fig.8.3 Closed Loop HBC with PI controller

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8.4.1 PI controller

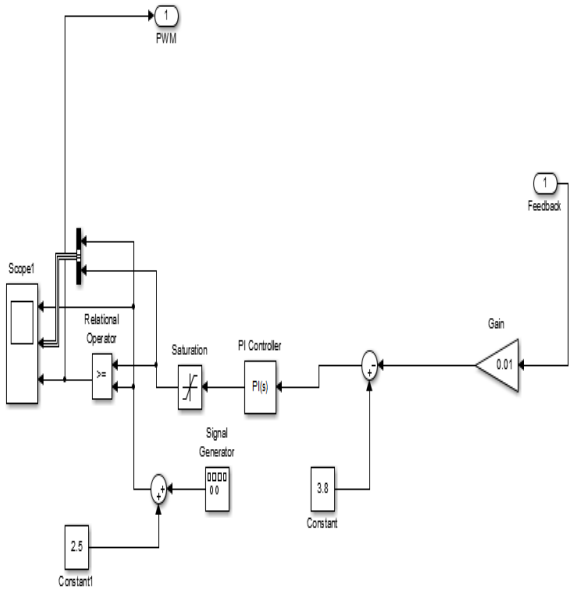

Fig8.4 PI controller of HBC

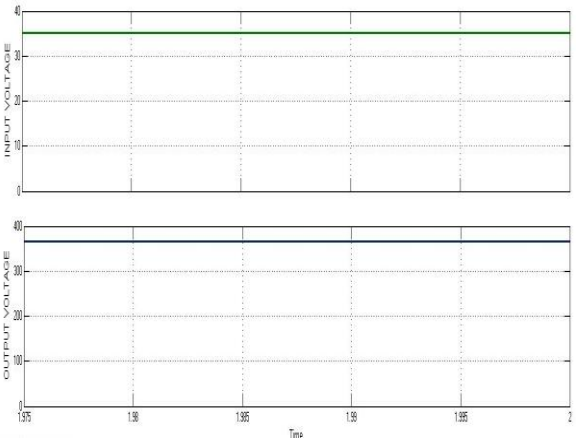

Fig 8.5 Input and Output of simulation using PI controlled System

8.4 Simulink Model of HBC with Fuzzy Controller

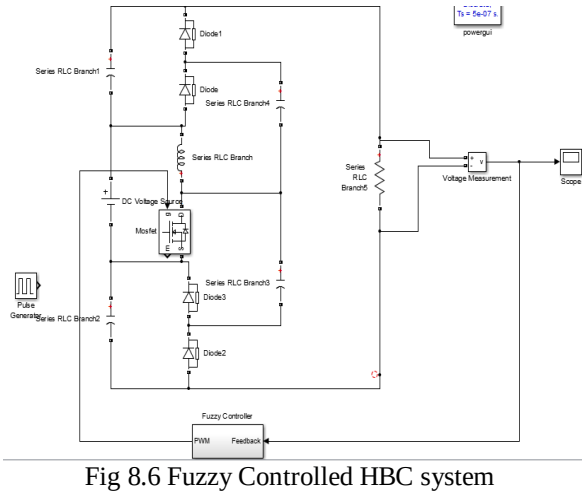

Fig 8.6 Fuzzy Controlled HBC system

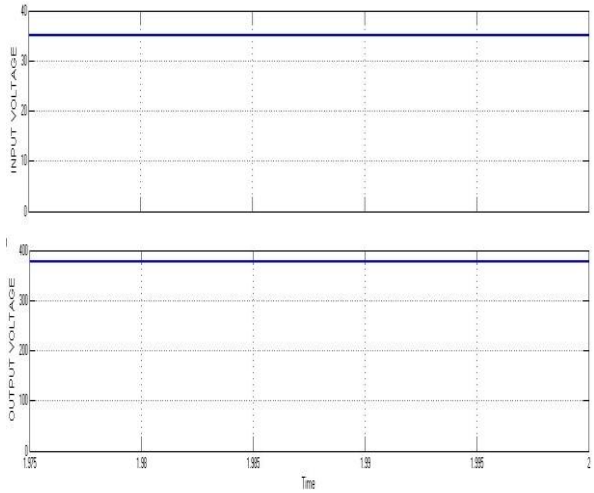

Fig 8.7 Output of Fuzzy Controlled system

IX. PERFORMANCE ANALYSIS

9.1. Component Stress Analysis

Detail analysis of components stress for the converter provides solid reference for components selection and optimization. The components stress under CCM mode is estimated in this section.

9.1.1) Diodes and Switch: According to the charge balance law of flying capacitors, all the diodes *Dia* (i = 1, 2, 3 . .2k) and *Dib* (i = 1, 2, 3 . . . 2k) have the same average current *IO* during one switching period. The average current during conduction state is used to calculate *I*rms here. The current waveforms of diodes and switch are shown in Fig. 11. Their current stress and voltage stress are listed in Table I.

TABLE I
COMPONENTS STRESS

	V_{max}	I_{ave}	I_{rms}
S	$\frac{V_{in}}{D'}$	$\frac{2kI_a}{D'}$	$2k\frac{I_O}{D'}\sqrt{D}$
$D_{ia}(i=1,3\ldots 2k-1)$			
$D_{ib}(i=2,4\ldots 2k)$	$\frac{V_{in}}{D'}$	-	$I_O\sqrt{\frac{}{}}$
$D_{ia}(i=2,4\ldots 2k)$			
$D_{ib}(i=1,3\ldots 2k-1)$	$\frac{V_{in}}{D'}$	I_0	$\frac{I_O}{\sqrt{D'}}$
C_{ia}	V_{in}	0	$I_O k\sqrt{\frac{1}{DD'}}$
$C_{ia}(i=3,5\ldots 2k-1)$	$\frac{V_{in}}{D'}$	0	$\left(k-\frac{i-1}{2}\right)I_O\sqrt{\frac{1}{DD'}}$
$C_{ib}(i=1,3\ldots 2k-1)$	$\frac{V_{in}}{D'}$	0	$\left(k-\frac{i-1}{2}\right)I_O\sqrt{\frac{1}{DD'}}$
$C_{ia}(i=2,4\ldots 2k)$	$\frac{V_{in}}{D'}$	0	$\left(\left(k-\frac{i}{2}\right)\frac{I_O}{D}+I_O\right)\sqrt{\frac{D}{D'}}$
$C_{ib}(i=2,4\ldots 2k)$	$\frac{V_{in}}{D'}$	0	$\left(\left(k-\frac{i}{2}\right)\frac{I_O}{D'}+I_O\right)\sqrt{\frac{D}{D'}}$

9.1.2) Capacitors: According to the analysis of BVM in Section II, the flying capacitors that are closer to inductive

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switching core have larger charging or discharging current, which exhibit larger voltage ripple. Their average charging and discharging current can be used to estimate the RMS current, which is useful to evaluate power loss of each capacitor. The expressions of RMS current for each capacitor in a 2kth-orderHBC are also given in Table I.

TABLE II
COMPARISON OF NORMALIZED CAPACITOR VOLTAGE STRESS FOR CONVERTER

Fig. 1	C1	C2	C3	C4	C5	Total
(a)	1/3	1/3	1/3	2/3	1	8/3
(b)	1/3	1/3	1/3	1/3	1/3	5/3
(c)	$\frac{1-D}{3-D}$	$\frac{2-D}{3-D}$	$\frac{1-D}{3-D}$	1	0	$\frac{8-4D}{3-D}$
(d)	1/3	1/3	1/3	1/3	1/3	5/3
(e)	1/2	1/2	1	0	0	2
(f)	$\frac{D}{1+D}$	$\frac{D}{1+D}$	1	0	0	$\frac{1+3D}{1+D}$
(g)	D/2	1/2	1	0	0	$\frac{3+D}{2}$
(h)	$\frac{1-D}{3-D}$	$\frac{1}{3-D}$	$\frac{1}{3-D}$	$\frac{1}{3-D}$	0	$\frac{4-D}{3-D}$

9.2 Voltage Ripple Analysis

The output voltage ripple is determined by the ripple of equivalent capacitor $C_{2a(eq)}$ and $C_{2b(eq)}$, assuming the input source has a constant voltage. As the equivalent capacitance of $C_{2a(eq)}$ and $C_{2b(eq)}$ are given as (21) and (26), the voltage ripple of $C_{2a(eq)}$ and $C_{2b(eq)}$ can be presented as following:

$$\Delta V_{c2a(eq)} = \frac{Io\ Ts}{2C} k(k - 1 + 2D) \qquad (47)$$

$$\Delta V_{c2b(eq)} == \frac{Io\ Ts}{2C} k(k - 1 + 2D') \qquad (48)$$

The final output ripple can be presented as following:

$$\Delta Vout = |\Delta V_{c2a(eq)} - \Delta V_{c2b(eq)}| = = \frac{Io\ Ts}{2C} k\ |2D - 1| \quad .(49)$$

According to the (47), when the duty cycle D is 0.5, the theoretical output voltage ripple is zero. The ripple examples of D = 0.8 and 0.5 are compared in Fig. 12(a) and (b). The interleaving operation has led to ripple cancelation of the capacitors $C_{2a(eq)}$ and $C_{2b(eq)}$.

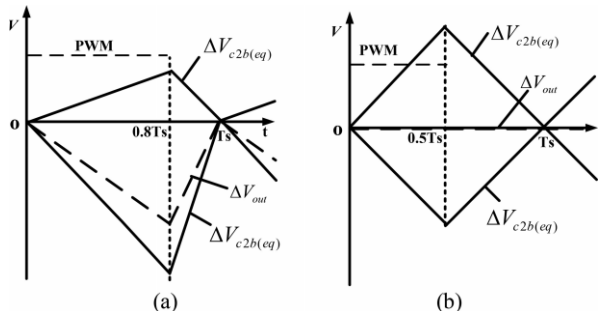

Fig.9.1 Voltage ripple cancellation with different duty cycle. (a) D = 0.8. (b) D = 0.5.

9.3 Comparison of Proposed HBC with Previous Converters

In order to distinguish the proposed HBC converter, a comparison is carried out between the second-order HBC converter and several previous published converters with single inductor and single switch shown in Fig. 1.1–1.6. All capacitors are assumed to have the same value C for easier comparison. The voltage gain, component count, as well as normalized switch stress and normalized output ripple are all listed for each topology in Table III. The absolute voltage gain curves for all topologies presented in Fig. 1 are sketched in Fig. 13. The proposed HBC has good gain boosting capability. However, it is difficult to judge the performance of each configuration merely based on the level of its gain curve, especially with consideration of different components count for different topologies. Most of the topologies can extend their gain by adding more stags with a larger number of capacitors and diodes. Therefore, more details should be taken into consideration to evaluate topologies, such as total normalized capacitor voltage rating and normalized output voltage ripple. For the high gain dc–dc converters with single switch and inductor, a critical aspect to realize high power density and lowcost is to decrease the physical size of capacitors.

Diodes usually have comparably much smaller volume, whose effect to the power density is neglected in this comparison. The voltage rating and capacitance value are the primary factors that affect the size of each capacitor. In order to compare the density of each topology with same gain, the normalized voltage stresses of capacitors for each topology are calculated in Table II. The normalized voltage stress for a capacitor is defined by the actual voltage stress of the capacitor divided by the output voltage *V*out. The total normalized capacitor voltage stress is the sum of all normalized capacitor voltage stress, which takes into account the capacitor number and voltage rating requirement. This parameter can be used to evaluate the size of high gain dc–dc converters with single switch and inductor.

The total normalized capacitor voltage stresses of all topologies are sketched in Fig. 14 based on results in Table II, with variation of duty cycle. Compared with other listed topologies, the proposed second order HBC has lowest total capacitor voltage stress in a wide range of duty cycle. This result shows the superiority of proposed structure for high power density design. In addition to the normalized capacitor voltage stress comparison, the normalized output ripple comparison is given in Fig. 15 according to Table III. Among all the converters considered, the proposed HBC structure (h) has the lowest ripple in the duty cycle range of [1/3, 2/3]. When duty cycle ranges are higher than 2/3, only converter (e) and (f) show smaller ripple theoretically. However, under this condition, converter (e) and (f) exhibits much larger normalized total capacitor voltage stress and weaker gain boosting capability, as shown in Figs. 13 and 14.

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It should be pointed out that although the proposed HBC structure has the advantages in high power density and low cost design, it also has the intrinsic issue of uncommon ground between source and load, which may limit its applications in areas where common ground are not required between input and output. Besides, due to direct connection between the input and output, the audio susceptibility may be an issue, which may require an input filter and fast control loop.

X. HARDWARE SETUP AND RESULTS

10.1 Introduction

The scaled downed hardware implementation of the Hybrid boost Converter is done .This chapter includes the experimental set up of the hardware and the hardware analysis. The components used to set up the power circuit and the controller details are also specified. The experimental results are included for the validation of the implemented system.

10.2 Block Diagram of Hardware

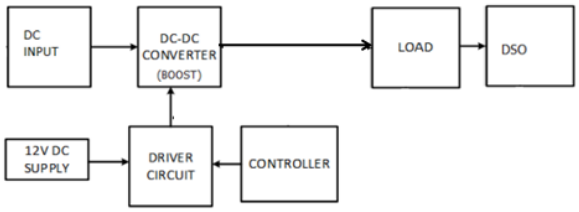

Fig 10.1 Hardware block diagram

Generally the whole system is composed of three parts

- Power circuit
- Controller
- Driver circuit

The power circuit consists of two parts, a dc –dc converter which is a boost converter and dc-ac converter which is a single phase seven level inverter. The controller is PIC16F877A for controlling the switching of the converter and inverter. A driver circuit is used in between the MOSFETs and the controller. The driver circuit used is a transistor driver. Power supply is provided for each of these components according to their requirements.

10.3 Components used in the hardware model

10.3.1 Controller-PIC16F877A

The term PIC stands for Peripheral Interface Controller .It is the brain child of Microchip Technology, USA. Originally this was developed as a supporting device for PDP computers to control its peripheral devices, and therefore named as PIC, Peripheral Interface Controller. They have coined this name to identify their single chip micro controllers. These 8-bit micro controllers have become very important now days in industrial automation and embedded applications etc.

Peripheral Interface Controllers (PIC) is a family of microcontrollers by microchip technology. Special features of this pic is listed below:

- 100,000 erase/write cycle Enhanced Flashprogram memory typical
- 1,000,000 erase/write cycle Data EEPROMmemory typical Data EEPROM Retention > 40 years
- Self-reprogrammable under software control
- Single-supply 5V In-Circuit Serial Programming
- Watchdog Timer (WDT) with its own on-chip RC
- oscillator for reliable operation
- Programmable code protection
- Power saving Sleep mode
- Selectable oscillator options
- In-Circuit Debug (ICD) via two pins
- 10-bit, up to 8-channel Analog-to-Digital
- Converter (A/D)
- Brown-out Reset (BOR)
- Inbuilt pwm module

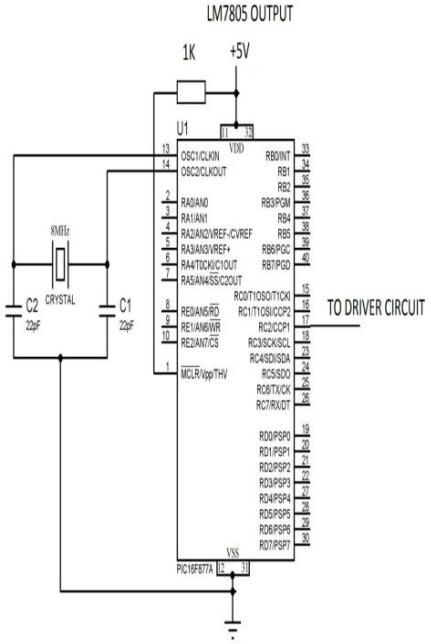

Fig 10.2 PIC connection diagram

10.3.2 Regulator IC LM7805

A voltage regulator is one of the most widely used electronic circuitry in any device. A regulated voltage (without fluctuations & noise levels) is very important for the smooth functioning of many digital electronic devices. A common case is with micro controllers, where a smooth regulated input voltage must be supplied for the micro controller to function smoothly.LM**7805** is a **voltage regulator** integrated circuit. It is a member of 78xx series of fixed linear voltage regulator ICs. The voltage source in a circuit may have fluctuations and would not give the fixed voltage output. The **voltage regulator IC** maintains the output voltage at a constant value. The xx in 78xx

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indicates the fixed output voltage it is designed to provide. 7805 provides +5V regulated power supply. Capacitors of suitable values can be connected at input and output pins depending upon the respective voltage levels.

10.3.3 IRFP250

This is a 200V, 33A, 0.085Ω Power MOSFET. This N-Channel enhancement mode silicon gate power field effect transistor is an advanced power MOSFET designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching convertors, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits .This MOSFET has high dv/dt capability, linear transfer characteristics and high input impedance

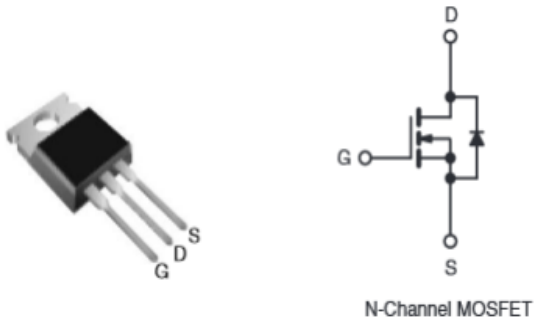

Fig10.3 Power MOSFET

10.3.4 Regulator IC LM7805

A voltage regulator is one of the most widely used electronic circuitry in any device. Pinout diagram of LM7805 regulator IC is shown in figure 6.3. A regulated voltage (without fluctuations & noise levels) is very important for the smooth functioning of many digital electronic devices. A common case is with micro controllers, where a smooth regulated input voltage must be supplied for the micro controller to function smoothly. LM7805 is a voltage regulator integrated circuit. It is a member of 78xx series fixed linear voltage regulator ICs.

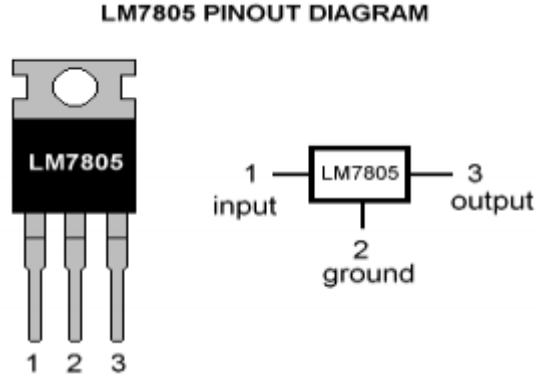

Fig10.4 Pinout diagram of LM 7805 regulator IC

The voltage source in a circuit may have fluctuations and would not give the fixed voltage output. The voltage regulator IC maintains the output voltage at a constant value. The xx in 78xx indicates the fixed output voltage it is designed to provide. 7805 provides +5V regulated power supply. Capacitors of suitable values can be connected at input and output pins depending upon the respective voltage levels.

10.4 Hardware Implementation

The experimental setup experimental setup is shown in figure 6.5.The converter input voltage is 3.4 V which is boosted to 35 V. The output voltage is measured across the load resistor. The output waveforms are analyzed with the help of DSO.

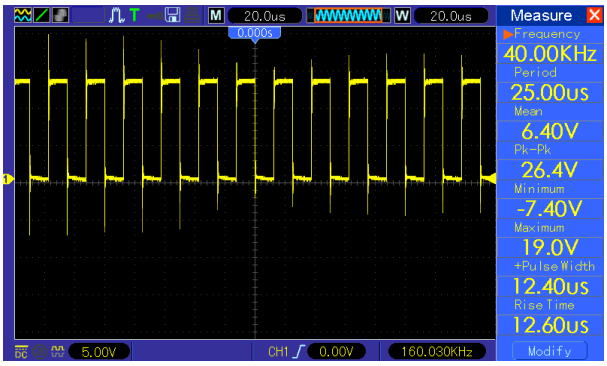

Fig10.7 Gate Pulse of HBC

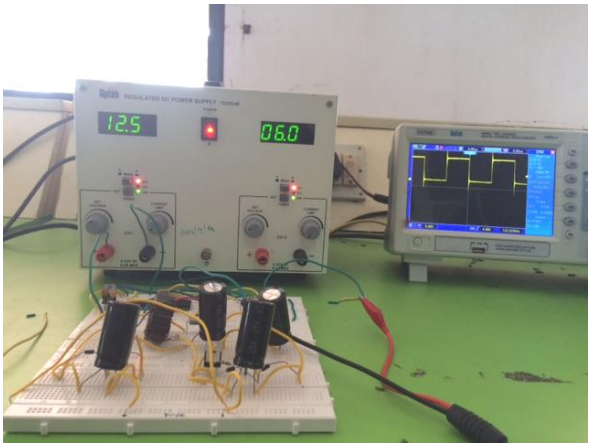

Fig10.5 Hardware Setup

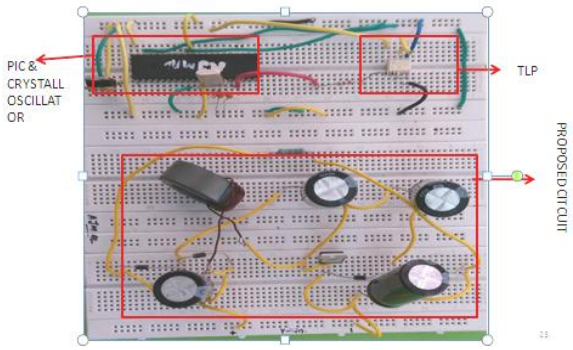

Fig.10.6 Hardware Prototype

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XI. CONCLUSION

A new HBC composed of an inductive switching core and BVM is proposed in this paper. The proposed converter has the collective advantages of the gain boosting technique from voltage multiplier and voltage regulation capability from boost converter, featuring in nature interleaved operation, wide regulation range, low component stresses, small output ripple, flexible gain extension, and high efficiency. Compared with other high gain boosting technologies such as tapped inductor, multi inductor/ switch method or transformer-based method, the proposed topology has reduced the complexity which is suitable for mass production. Compared with other single switch and utilization rate, smaller output ripple and lower component stress. This paper provides operation principle, design consideration,and overall comparison with many other similar topologies.single inductor dc–dc converters, it has a better component

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BIOGRAPHIES

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